

13JA2000

REC'D. - WMA
JAN 14 2000

REC'D. - WMA
JAN 14 2000
5204 E. Ben White Blvd.
Austin, TX 78741
Tel (512) 385-8542

J. MIKE AMERSON
WILLIAMS, MORGAN & AMERSON
7676 HILLMONT, SUITE 250
HOUSTON, TX 77040

RE: Invention Disclosure TT3851

Entitled:

IMPROVED DOF FOR TFVL VIA-PROCESSING WITH HARDMASK AND LOW VISCOSITY RESIST

Dear J. MIKE AMERSON:

2000.046600

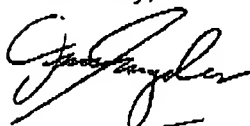
Please prepare a US patent application for the subject invention disclosure and file the application in the USPTO within two months of this letter. A copy of the Invention Disclosure is enclosed.

Please follow the instructions set forth in AMD's DIRECTIONS TO OUTSIDE COUNSEL REGARDING PREPARATION AND PROSECUTION OF PATENT APPLICATIONS Version 1.0 dated May 1, 1996.

It is not necessary to prepare a PCT international application at this time. If one is later determined to be needed, AMD will so advise you.

If you have any questions or need additional information, please call me at 512-602-5964, or the responsible AMD Technology Law attorney, PAUL S. DRAKE at 512-602-2103.

Sincerely,



Samantha Cardona
Paralegal
Technology Law Department

Enclosure

cc:

TSUI, TING YIU
PARK, STEVEN KEETAJ 24527 (CA)

BEST AVAILABLE COPY

EXHIBIT A

AMD INVENTION DISCLOSURE

TLD ID#

773857

Rec'd date

Sunnyvale x42110, return to MS68.

Texas x55964 return to MS62

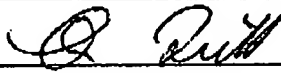
Project: ☐, Product: ☐, Process: ☒, Technology ☐, to which the invention applies (identify):

Product, Process, Technology

List 2 to 5 key words useful to search by to find patents or art related to this invention:

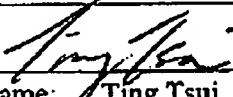
Surface Chemistry Modification, Lithography, Trench first Via last processingWorking title of invention: Improved DOF for TFLV Via-processing with hardmask and low viscosity resist.

Inventor's signature:

date: 10/20/99Inventor's printed full name: Christian Zistl Citizenship: GermanyEmployee #: 200202 Extension: 512 933 2456 Mail stop: K-10 Home telephone: (512) 892 6861Division: Fab30 Directorate: Fab30 Dept #: 7045 Dept: Integration Manager: Michael RaabResidence address: 5800 Brodie Lane #233, Austin TX, 78745 (after 11/18/99: Markusstr.18, 01149Dresden, GERMANY, work phone: +49 351 277 4537)

Post Office address:

Co-Inventor's signature:

date: 10/20/99Co-Inventor's printed full name: Ting Tsui Citizenship: Hong KongEmployee #: 24378 Extension: 512 933 6364 Mail stop: K-10 Home telephone: (512) 416-8910Division: ALT Directorate: TDG Dept #: 7983 Dept: ALT Manager: Steve ZikaResidence address: 1104 Misson Ridge, Austin TX, 78704

Post Office address:

Co-Inventor's signature:

date: 10/24Co-Inventor's printed full name: Stephen Keetal Park Citizenship: KoreaEmployee #: 24527 Extension: 933 2557 Mail stop: K-10 Home telephone: (512) 899-9496

Division: _____ Directorate: _____ Dept #: _____ Dept: _____ Manager: _____

Residence address: 5701 Mopac Way #626, Austin TX, 78721

Post Office address:

Co-Inventor's signature:

date: _____

Co-Inventor's printed full name: _____ Citizenship: _____

Employee #: _____ Extension: _____ Mail stop: _____ Home telephone: () _____

Division: _____ Directorate: _____ Dept #: _____ Dept: _____ Manager: _____

Residence address: _____

Post Office address: _____

List on additional sheet if there are more co-inventors and list total number of inventors here: _____

Name(s) of attorney(s) preferred by inventor(s) to prepare patent application, if known: DO NOT SIGNWitness 1 initial: SLWitness 2 initial: SL

AMD CONFIDENTIAL

Page 1

AMD INVENTION DISCLOSURE

TLD ID# _____

Rec'd date _____

Sunnyvale x42110, return to MS68,

Texas x55964 return to MS62

Identify known relevant art (patents, publications, products): _____

Cu dual damascene process.

Trench first via last (TFVL) approach is the most typical process flow since TFVL is relatively easier than VFTL (via first trench last) approach to process.

State the problem solved by this invention: _____

Improves the common depth of Focus at the via photo level for Dual Damascene with trench first via last processing scheme. Additionally the interlayer capacity is reduced.

Brief description and/or sketch of invention (please attach copies of AMD patent notebook pages, reports or drawings): _____

During standard processing of dual damascene structures with the trench first via last approach Via photo faces always the problem of varying resist thickness.

In the process scheme of TFVL (trench first via last) one etches first the trenches, which will be the metal lines, spin resist on this structured wafers for the via process and expose this resist.

With this scheme the resist thickness from resist top to trench bottom in isolated lines is always higher than in wide lines, which are typically more than 20times at wide minimal lines (a typical variation can be seen in fig.1 where the x direction is shown compressed).

This rises a problem for photo during the Via Photo process, because the different resist thickness lead to a different optimal focus setting for varying structures. So the region of common depth of focus (DOF) is reduced with this resist thickness variation to a degree that there may be no common DOF left for all different structures. This may lead to missing vias, since they are not printed.

The optimum for exposing resist would be a flat resist all over the wafer.

This invention explains how to reach almost uniform resist thickness all across all different structures.

A resist-thickness-variation of almost 0 can be reached with a low viscosity photo resist. With such a resist it is possible to fill all trench structures and have a small resist thickness on unstructured areas. The resist thickness on unstructured parts of the wafer should be smaller or around 0.5 of the trench-depth. So the thickness variation between unstructured part of the wafer and areas with high trench density can be reduced dramatically (Fig.2). So the surface of the resist for the Via exposure is almost flat using this technique.

In order to give etch the possibility to etch the vias with a very thin resist the use of a hard mask on top of the ILD is necessary. (For a SiO₂ like ILD SiON is a possible choice for a hard mask and for low k materials a standard TEOS layer can be used). This hard mask can also be used as a top ARC and removes the requirement of a bottom ARC in the ILD stack. Fig 3 shows a principle picture of a wafer after via etch using this technique. Further standard processing is done after that (barrier deposition, Cu fill and Cu Polish). Fig 4

Witness 1 initial: _____

Witness 2 initial: _____

AMD CONFIDENTIAL

Page 2

AMD INVENTION DISCLOSURE

TLD ID#

Rec'd date

Sunnyvale x42110, return to MS68,

Texas x55964 return to MS62

During the Cu-polish step the hard mask will be removed. This has an additional advantage if the hard mask was used as a top ARC. In that case you can get rid of one ILD layer with high dielectric constant, what will reduce the effective k of the ILD stack.

Endresult is a dual damascene structure without an ILD layer with high dielectrical constant.

Patent notebook # _____ Page numbers _____ Number of drawings _____

Witness 1 initial: SL Witness 2 initial: [Signature]

viaDOF.doc DB 7/31/05 printed 10/20/99 1:08 PM dncc rev 11/25/96

AMD CONFIDENTIAL

Page 3

AMD INVENTION DISCLOSURE

TLD ID# _____

Rec'd date _____

Sunnyvale x42110, return to MS68.

Texas x55964 return to MS62

Advantages (check all that apply):

<input type="checkbox"/> avoids existing patent(s)	<input checked="" type="checkbox"/> improves precision	<input checked="" type="checkbox"/> simplifies manufacturing
<input checked="" type="checkbox"/> new function	<input checked="" type="checkbox"/> improves accuracy	<input type="checkbox"/> improves wear characteristic
<input type="checkbox"/> improves density	<input type="checkbox"/> improves efficiency	<input type="checkbox"/> improves signal to noise ratio
<input type="checkbox"/> increases operating speed	<input type="checkbox"/> fewer component parts	<input type="checkbox"/>
<input type="checkbox"/> improves reliability	<input type="checkbox"/> reduces cost of manufacturing	<input type="checkbox"/>

Discussion of advantage of the invention over other solutions

(emphasize technical advance in the art as measured against known art): _____

First written description* of invention, date:	First external disclosure to (name):
Date of first drawing*:	Date of first external disclosure, none <input type="checkbox"/>
Date invention first reduced to practice:	External disclosure under NDA* No <input type="checkbox"/> Yes <input type="checkbox"/>
Made by (name):	First external disclosure or use by: presentation <input type="checkbox"/> ,
Tested by (name):	announcement <input type="checkbox"/> , sample <input type="checkbox"/> , sale <input type="checkbox"/> , other <input type="checkbox"/>
Date of first computer simulation:	Date of Non-Disclosure Agreement*, if any:
Date of first successful test:	Date of first publication*:
any of above occurred outside of USA <input type="checkbox"/>	Publication name:
* attach copy if possible	Date of first commercial use:

Does plan exist to publish, disclose or sell? If so, where and when? _____

Was invention conceived, constructed or tested pursuant to the performance under a development contract with another company: No ☒, Yes ☐. If yes, company name _____

If yes, name of AMD business contact and contract no. _____

Was invention jointly developed with participation of inventors from outside AMD: No ☒, Yes ☐.

If yes, Company name _____

I have read and understood this disclosure and read and signed each page of the attachments:

Witness 1 signature: Scott Luning Date: 10/20/99
 Printed name: Scott Luning Employee #: 23152

Witness 2 signature: John M. ... Date: 10/20/99
 Printed name: John M. ... Employee #: 64243

After completing to this point, deliver to department reviewer: date delivered _____

Witness 1 initial: SL Witness 2 initial: JM

VRDOF:00C DB 7/31/05 printed: 11/21/04 1:04 PM nppp rev 11/25/05

AMD CONFIDENTIAL

Page 4

AMD INVENTION DISCLOSURE

TLD ID#

Rec'd date

Sunnyvale x42110, return to MS68.

Texas x55964 return to MS62

DISCLOSURE EVALUATION (Entries from this point on are by the Reviewer)Does this invention add value to the AMD intellectual property portfolio? Yes ☒ No ☐

Explain:

better DoF @ e-tho. Improved process window

Do you know of any relevant art? Yes ☐ No ☒ If yes, attach a copy and explain:

What application(s) do you foresee for this invention?

HIP7, HIP8, CS68

I estimate the Value* of this invention disclosure is A ☐ B ☐ C ☐ D ☐

*use worksheet "Valuing Invention Disclosures and Patents".

it is ☒ is not ☐ recommended to AMD for U.S. patent application filing.it is ☐ is not ☒ recommended to AMD for foreign patent application filing.it is ☐ is not ☒ recommended to be held as an AMD trade secret.Give this high priority ☐ normal ☒ low priority ☐ in patent application writing.***GUIDELINES AND CONSIDERATIONS FOR FOREIGN FILING DECISION***

Filing foreign patent applications is costly. We should choose to do it only when conditions warrant.

ALL CONDITIONS BELOW MUST APPLY IN ORDER TO INITIATE A FOREIGN FILING:

- Invention is High-Valued (A, B)*, and
- Invention is in our technology path (usage), and
- Invention usage is detectable by inspection of product, and
- Invention is relatively hard to design around, and
- Competitor is operating in the country of interest. (see ca000000.xls tabulation of "Factory Sites outside the USA .)

I recommend filing patent applications in foreign countries checked below:

Japan: <input type="checkbox"/>	S.Korea <input type="checkbox"/>	Taiwan <input type="checkbox"/>	U.K. <input type="checkbox"/>	France <input type="checkbox"/>	Germany <input type="checkbox"/>
<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>

Reviewer's signature:

Paul Besser

Employee #:

23186

Date:

10/27/99

Reviewer's printed name:

Paul Besser

If foreign filing is checked, route to Div. VP for signature.

VP or Designate approves foreign filing (signature)

Reviewer: Complete this page and send (all) disclosures to TLD, including those not recommended for patent application filing.

Fig.: 1

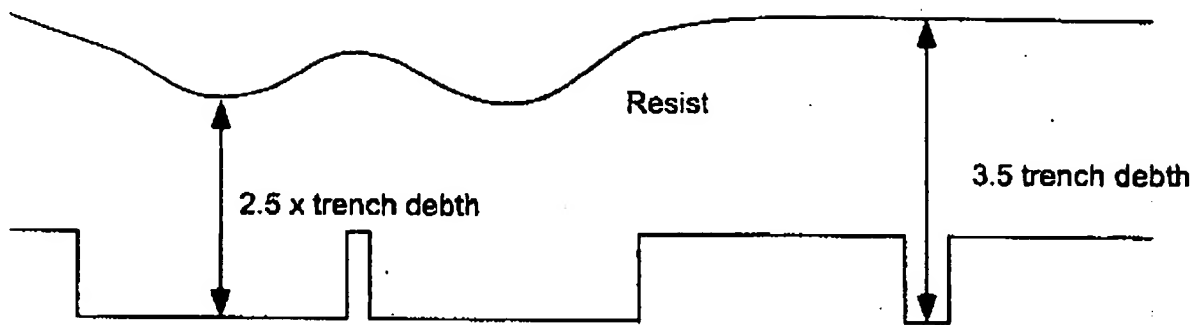


Fig. : 2

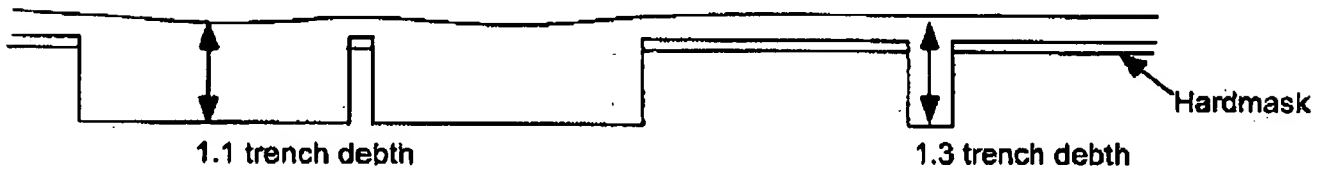


Fig.3:

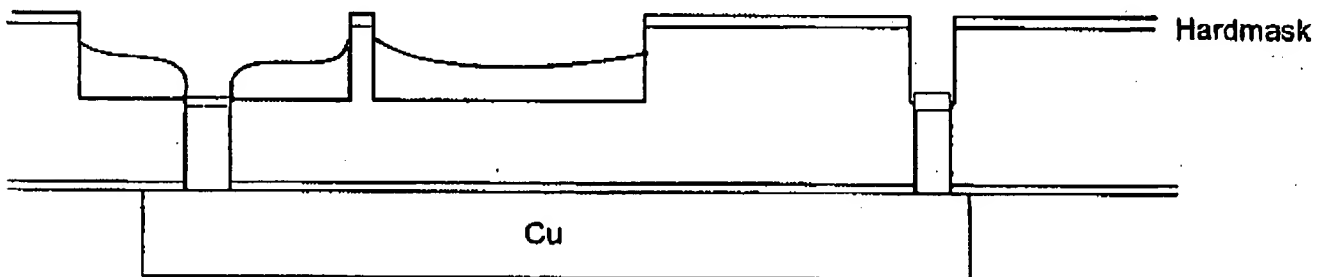
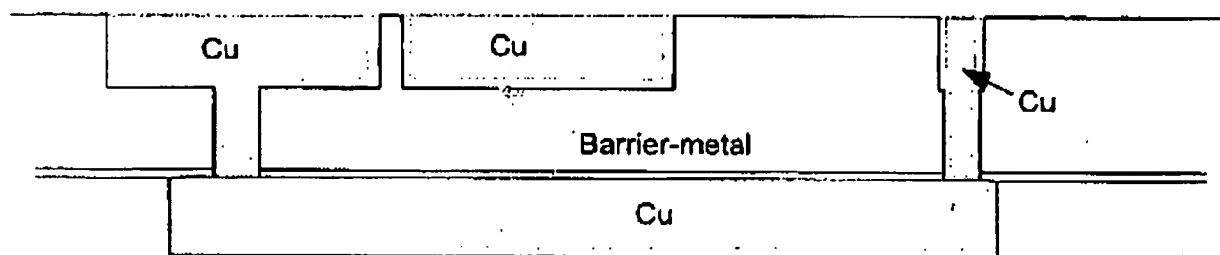


Fig.4:



**This Page is Inserted by IFW Indexing and Scanning
Operations and is not part of the Official Record**

BEST AVAILABLE IMAGES

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images include but are not limited to the items checked:

- ☐ **BLACK BORDERS**
- ☐ **IMAGE CUT OFF AT TOP, BOTTOM OR SIDES**
- ☐ **FADED TEXT OR DRAWING**
- ☐ **BLURRED OR ILLEGIBLE TEXT OR DRAWING**
- ☐ **SKEWED/SLANTED IMAGES**
- ☐ **COLOR OR BLACK AND WHITE PHOTOGRAPHS**
- ☐ **GRAY SCALE DOCUMENTS**
- ☐ **LINES OR MARKS ON ORIGINAL DOCUMENT**
- ☐ **REFERENCE(S) OR EXHIBIT(S) SUBMITTED ARE POOR QUALITY**
- ☐ **OTHER:** _____

IMAGES ARE BEST AVAILABLE COPY.

As rescanning these documents will not correct the image problems checked, please do not report these problems to the IFW Image Problem Mailbox.